IN THE SPECIFICATION

Please replace the section of the application entitled "Brief Description of the Drawings" that begins on page 4 of the application with the following rewritten section:

Brief Description of the Drawings

Fig. 1 is a schematic diagram for explaining a problem in a ~~photo process;~~ photo process.

Fig. 2 is a schematic diagram for explaining a problem in an ~~etching process;~~ etching process.

Fig. 3 is a block diagram for illustrating the layout of an embodiment of a conventional semiconductor ~~memory device;~~ memory device.

Fig. 4 is a circuit diagram of a conventional ~~sense amplifier;~~ sense amplifier.

Fig. 5 illustrates the layout of sources, drains and gates of the transistors which make up the sense amplifier.

Fig. 6 illustrates contacts formed in the layout shown in Fig. 5.

Fig. 7 illustrates metals formed at the contacts shown in Fig. 6.

Fig. 8 illustrates contacts formed at the metals shown in Fig. 7.

Fig. 9 illustrates metal lines formed along with the contacts shown in Fig. 8.

Fig. 10 illustrates metals for applying power voltage and grounding voltage to the metal lines.

Fig. 11 is a diagram for illustrating the layout of the sense amplifier shown in Fig. 4 in accordance with a layout method of an embodiment of the ~~present invention;~~ present invention.

Fig. 12 illustrates a layout method of the sense amplifier as shown in Fig. 4 in accordance with an embodiment of the present invention.

Fig. 13 illustrates contacts formed in the layout shown in Fig. 12.

Fig. 14 illustrates metals formed at the contacts shown in Fig. 13.

Fig. 15 illustrates contacts formed at the metals shown in Fig. 14.

Fig. 16 illustrates metal lines formed along with the contacts shown in Fig. 15.

Fig. 17 illustrates a power voltage applying line and a grounding voltage applying line.

Fig. 18 is a graph for illustrating variances of process deviations in accordance with the conventional layout method and the layout method of the present invention.